AMENDMENTS TO THE SPECIFICATION

Please amend the Specification as follows:

On page 1, under the names of the inventors, please add:

This application is a continuation of U.S. Patent Application Serial No. 10/346,584, filed January 17, 2003, which is a continuation of U.S. Patent Application Serial No. 09/939,977, filed August 27, 2001, now U.S. Patent No. 6,570,513, which is a continuation of U.S. Patent Application Serial No. 09/792,940, filed February 26, 2001, now U.S. Patent No. 6,297,755, which is a continuation of U.S. Patent Application Serial No. 09/460,444, filed December 13, 1999, now U.S. Patent No. 6,225,927, which is a continuation of U.S. Patent Application Serial No. 09/316,808, filed May 21, 1999, now U.S. Patent No. 6,107,948, which is a continuation of U.S. Serial No. 09/226,253, filed January 7, 1999, now U.S. Patent No. 6,191,717, which is a continuation of U.S. Serial No. 08/837,702, filed April 22, 1997, now U. S. Patent No. 5,870,046.

On page 7, replace lines 23-24 with:

Figures 6A and 6B are ~~is a~~ schematic diagrams of the active diode bridge circuit that is used as a power supply in preferred embodiments of the present invention.

On pages 23-24, replace the paragraph from lines 24-33 and 1-7 with:

A preferred embodiment of frequency detector 818 is shown in Figure 10. The inputs to frequency detector 818 are the DATA and CK4 signals and the outputs are the SPEED-UP2 and SLOW-DOWN2 signals. Delay cell 880 has its input connected to CK4 and output connected to one input of NOR gate 882. The delay cell 880 consists of an even number of capacitively loaded inverter stages or other delay generating circuitry and is well known in the art. The output of inverter 884 is connected to the other input of NOR gate 882 and the input of inverter 884 is connected to CK4. The output 886 of NOR gate 882 is reset pulse that occurs on the rising edge of CK4, and is connected to the reset input of D flip-flops 888, 890, and 892. The

input of inverter ~~894~~ 895 is connected to DATA. The output of inverter ~~894~~ 895 is connected to the clock input of D flip-flops 888, 890, and 892. The D input of flip-flop 888 is connected to V_{DD}. The D-input of flip-flop 890 is connected to the Q-output of flip-flop 888. The D- input of flip-flop 892 is connected to the Q-output of flip-flop 890. D flip-flops 894 and 896 have their clock inputs connected to CK4. The D input of flip-flop 894 is connected to the Q output of flip-flop 888. The D-input of flip-flop 896 is connected to the Q-output of flip-flop 890. The input of inverter 898 is connected to the Q-output of flip-flop 894, and the output of inverter 898 is the SLOW-DOWN2 signal. OR gate 900 provides the SPEED-UP2 signal. One input of OR gate 900 is connected to the Q-output of flip-flop 896, and the other input is connected to the Q-output of flip-flop 892. The SPEED-UP2 and SLOW-DOWN2 signals are connected to the frequency-detector charge pump 824.